Z80 CPU Board V2.1 - Default Jumper Settings

JP1, JP2, JP3 No jumper. These may be connected to provide extra ground lines on board IF ALL boards meet IEEE-696 specs

JP4 Connected. This puts a “power on clear” signal to the S-100 POC

JP5 No jumper. When jumpered, connects a capacitor to the S-100 RESET line.

JP6 Connected. This puts a “power on reset” signal to the S-100 SLAVE_CLEAR*

JP7 Connected. This puts a “power on reset” signal to the S-100 RESET*

JP8 Connect bottom two pins (1-2). This connects A11 to 27C64 boot ROM.

JP9 No jumper. This leaves pin 26 on the 27C64 boot ROM (designed to be a no-connect) floating.

JP10 Connected. Required to enable the on-board boot ROM.

K1 No jumper. Only to be used when NMI software has been implemented.

K2 Connect top two pins (2-3). Controls tri-stating of S100 bus control signals. Some older non-IEEE 696 S-100 boards (eg Cromemco Dazzler) may require connecting bottom two pins (1-2).

K3 Connect bottom two pins (1-2). This connects the on-board CPU clock oscillator to the Z80.

P2

```
7       8
5       6
3--------4
1       2
```

Horizontally connect second pair of pins from the bottom (3-4). This sets the memory window configuration port to D0h

P3 No jumpers. This sets the boot ROM address to F000h

P4

```
1       3
|       |
2       4
```

Vertically connect the two pairs of pins. Pair 1-2 connects the on-board 2MHz oscillator to the S-100 bus. Pair 3-4 connects the on-board MWRT signal to the S-100 bus.

P8, P9, P10

```
P10     P8      P9
4--------4      4
3--------3      3
2--------2      2
1--------1      1
```

Horizontally connect all 4 pairs of P10 and P8 pins. This connects A12-A16 to the comparator that performs boot ROM address selection.

P36

```
5       6
3--------4
1       2
```

Horizontally connect the middle pair of pins, which applies wait states only for M1 memory bus cycles.
Pair 5-6 will apply wait states on all memory bus cycles.
Pair 1-2 will apply wait states on all sINTA cycles.
The number of wait states for all three options is set by SW2.

P37

```
1       3

2       4
```

No jumpers.
Jumper 1-2 selects for “Partial Latch” mode of address and status signals on S100 bus. “Partial Latch” mode that does not adhere to IEEE-696 standard, and is usually not required. “Partial Latch” mode is not compatible with use of this board’s bank switching feature and CPM3.

P39

```
1       2
3       4
5       6
7--------8
```

Horizontally connect the bottom pair of pins. This allows the monitor software to select either the bottom or top 4K of the 8K boot ROM memory space. Note the pin numbering does not follow the same convention (ie numbers increment from the bottom up) as for other jumper pins on this board.